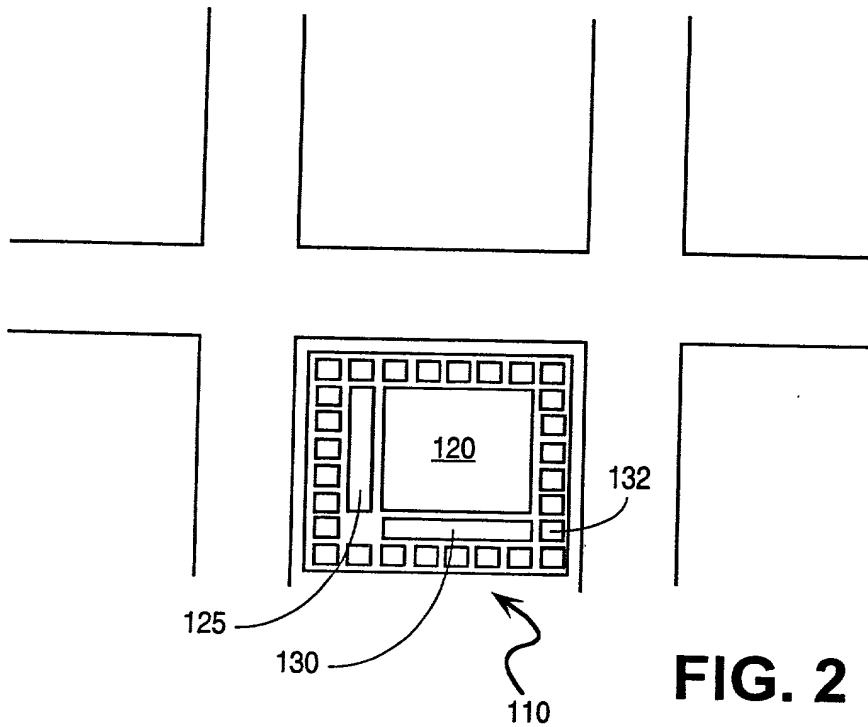
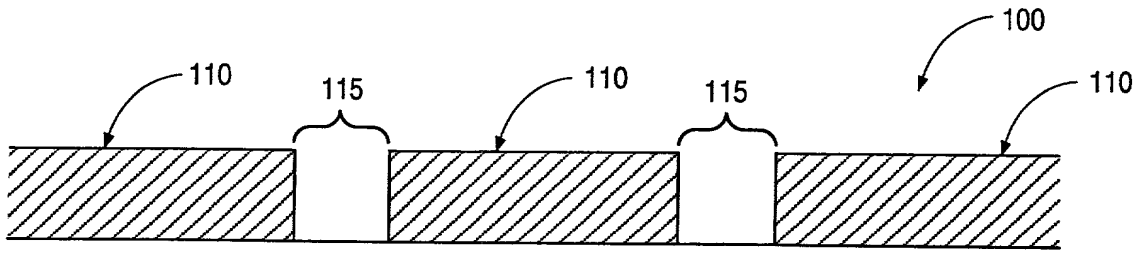


**FIG. 1**

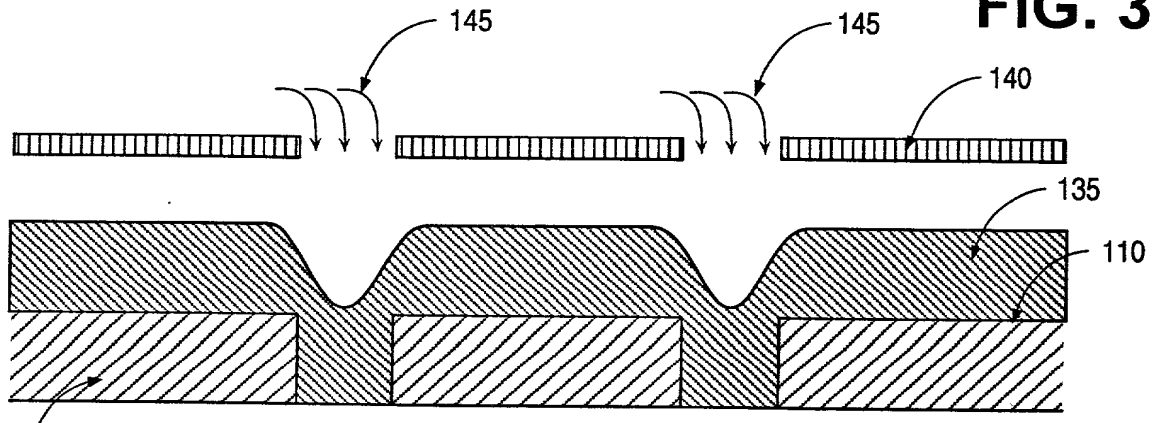


**FIG. 2**

This drawing is a schematic representation of a device and is not intended to be a true-to-scale drawing. The dimensions and proportions are not necessarily to scale.

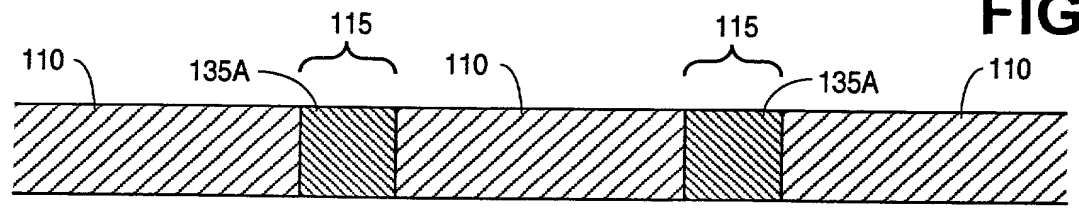


**FIG. 3**

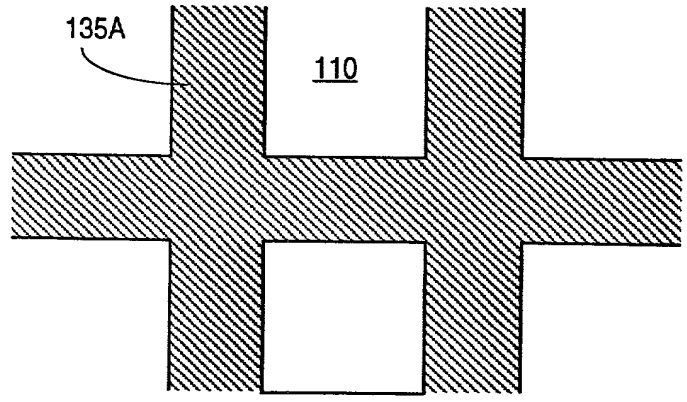


110

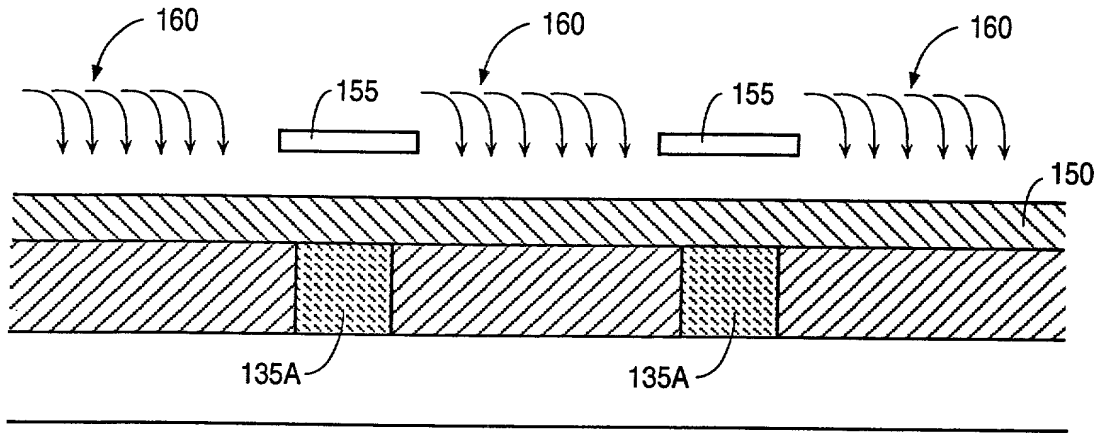
**FIG. 4**



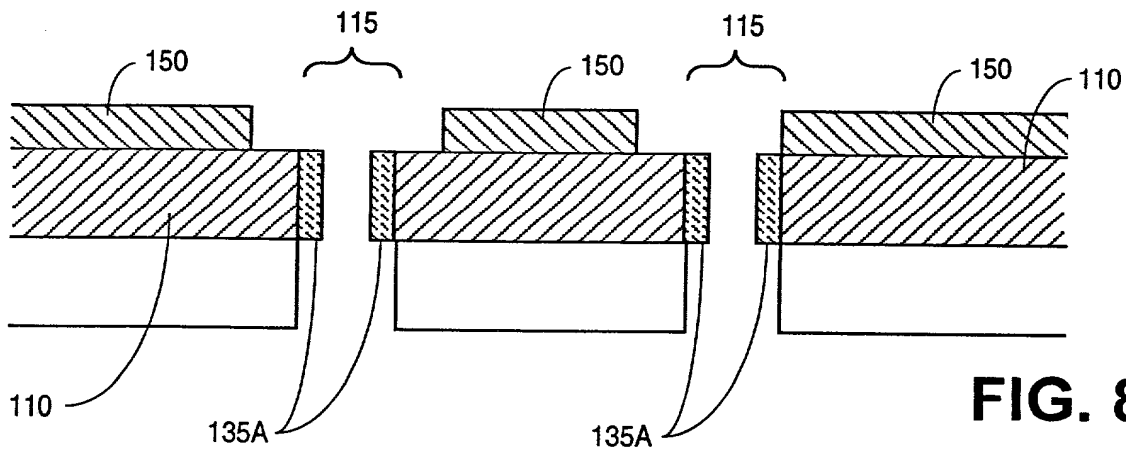
**FIG. 5**



**FIG. 6**

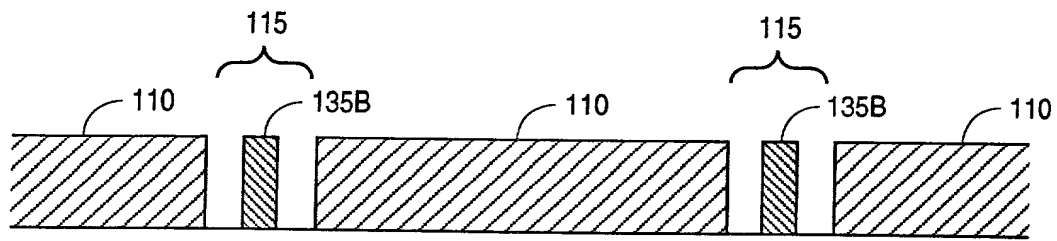


**FIG. 7**

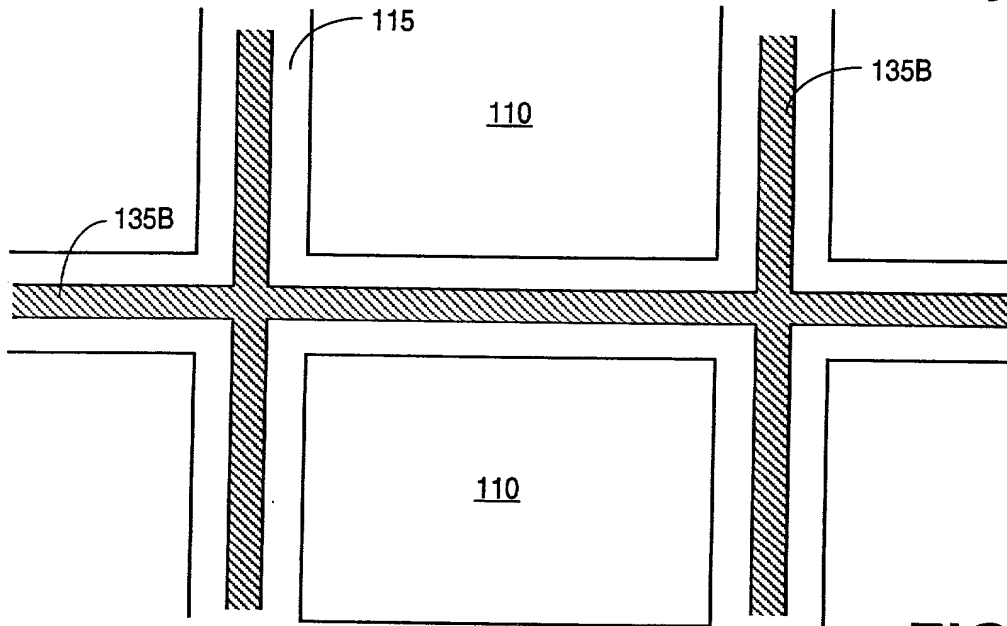


**FIG. 8**

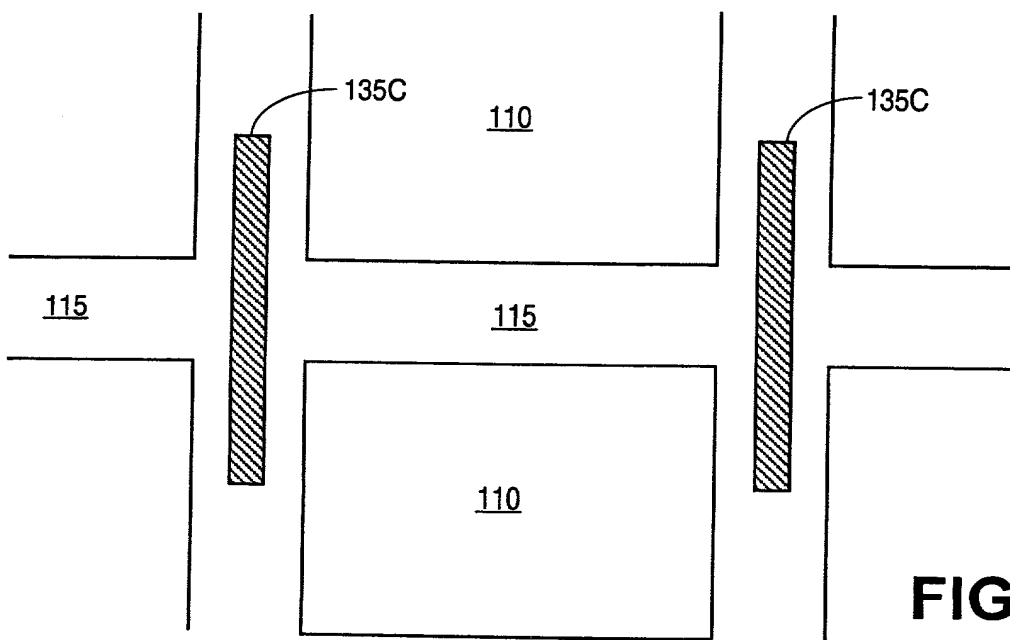
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**FIG. 9**



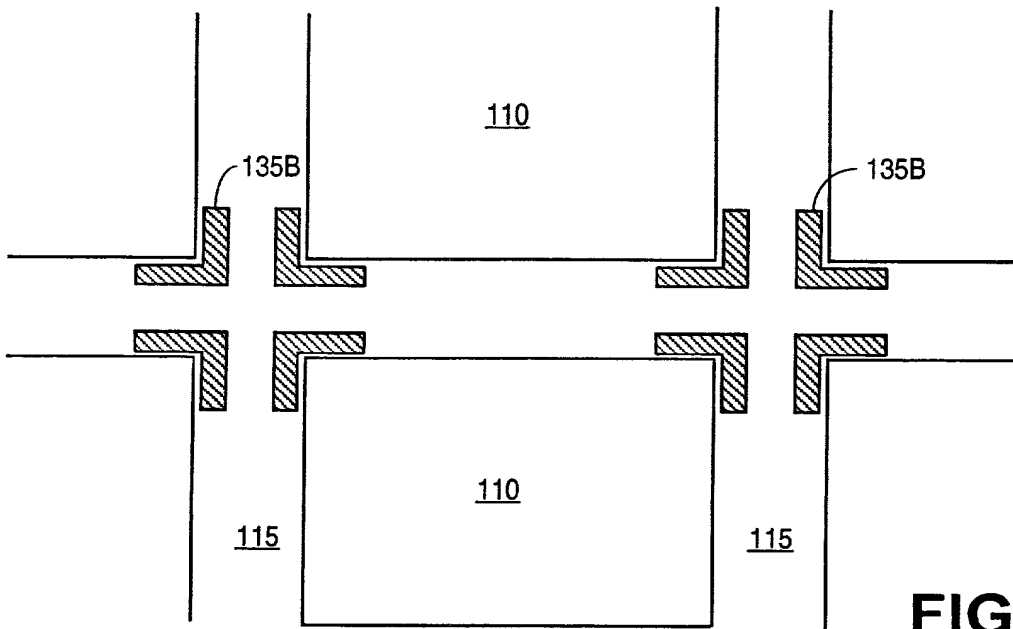
**FIG. 10**



**FIG. 11**

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FIG. 12 is a cross-sectional view of a device in accordance with the present invention. The device includes a substrate 110, a gate dielectric layer 115, and a gate electrode 135B. The gate electrode 135B is positioned over the gate dielectric layer 115 and is electrically connected to a gate terminal. The substrate 110 is electrically connected to a source terminal and a drain terminal. The device is formed on a substrate 110 and includes a gate dielectric layer 115 and a gate electrode 135B. The gate electrode 135B is positioned over the gate dielectric layer 115 and is electrically connected to a gate terminal. The substrate 110 is electrically connected to a source terminal and a drain terminal.



**FIG. 12**